Reg No.:_____ Name:_____

APJ ABDUL KALAM TECHNOLOGICAL UNIVERSITY

THIRD SEMESTER B.TECH DEGREE EXAMINATION(R&S), DECEMBER 2019

Course Code: CS203

Course Name: SWITCHING THEORY AND LOGIC DESIGN

Max. Marks: 100 Duration: 3 Hours

PART A

Answer all questions, each carries 3 marks. Marks

1 What is the largest binary number that can be expressed with 16 bits? What are the equivalent decimal and hexadecimal numbers? (3)

2 Perform subtraction on the given unsigned binary numbers using the 2's complement of the subtrahend. Where the result should be negative, find its 2's complement and affix a minus sign. (3)

(i) 10011 - 10010 (ii) 100010 - 100110

3 Find the complement of the following expressions: (3)

(i) xy' + x'y (ii) (a + c) (a + b') (a' + b + c')

4 State and Prove Absorption law in Boolean Algebra. (3)

PART B

Answer any two full questions, each carries 9 marks.

5 (a) The value of a float type variable is represented using a single precision 32 bit floating point format IEEE 754 standard that uses 1 bit for the sign , 8 bits for biased exponent and 23 bits for the mantissa. A float type variable X is assigned value of -0.0625 .What is the representation of X in hexadecimal notation? (6)

(b) Perform the following operations (3)

(i) Find the 16's complement of C3DF.

(ii) Convert C3DF to binary.

(iii) Find the 2's complement of the result in (ii)

6 (a) Add and multiply the following numbers without converting them to decimal. (6)

(i) Binary numbers 1011 and 101.

(ii) Octal numbers 62 and 37

(iii) Hexadecimal numbers 2E and 34.

(b) Represent the unsigned decimal numbers 791 and 658 in BCD, and then show the steps necessary to form their sum. (3)

7 (a) We can perform logical operations on strings of bits by considering each pair of corresponding bits separately (called bitwise operation). Given two eight- bit strings A = 10110001 and B = 10101100, evaluate the eight- bit result after the following logical operations: (3)

(i) AND (ii) OR (iii) XOR

(b) Simplify the following Boolean expressions to a minimum number of literals: (6)

(i) x'yz + xz (ii) (x + y) (x + y') (iii) xyz + x'y + xyz'

PART C

Answer all questions, each carries3 marks.

8		Design a combinational circuit with three inputs and one output. The output of the circuit is 1 when the decimal value of the inputs is less than 3. The output is 0 otherwise.	(3)
9		Implement the Boolean function **F(A, B, C, D) = π(3, 7, 12)** with a multiplexer:	(3)
10		Differentiate between Combinational and Sequential circuits. Give two examples for each.	(3)
11		Construct a JK flip-flop using a D flip-flop, a two-to-one-line multiplexer, and an inverter.	(3)

PART D

Answer any two full questions, each carries9 marks.

12	(a)	Design a four-bit 2's complementer combinational circuit. The circuit accepts a 4-bit binary number as input and generates the 2's complement of the input. Show that the circuit can be constructed with exclusive-OR gates.	(7)
	(b)	Predict what the output functions are for a five-bit 2's complementer?	(2)
13	(a)	Show that the characteristic equation for the complement output of a JK flip-flop is: $Q'(t+1) = J'Q' + KQ$	(3)
	(b)	Draw the logic diagram of a 4x16 decoder constructed with two 3x8 decoders	(4)
	(c)	Implement T flip- flop using NAND gates.	(2)
14		A sequential circuit has two JK flip-flops A and B and one input x . The circuit is described by the following flip-flop input equations: $J_A = x$ $K_A = B'$ $J_B = x$ $K_B = A$ (i) Tabulate the state table. (ii) Draw the state diagram of the circuit. (iii) Derive the state equations for A(t+1) and B(t+1)	(9)

PART E

Answer any four full questions, each carries10 marks.

15	(a)	Draw and explain the different types of shift registers.	(6)
	(b)	Explain how shift registers can be used for serial transfer.	(4)
16		Design and construct a Johnson counter with 8 distinguishable states. Give its timing diagram.	(10)
17	(a)	Design a synchronous counter with the following repeated binary sequence 000, 100,111, 010, 011 using T Flip Flops.	(6)
	(b)	Write a note on error detection and correction.	(4)
18		Find the minimum size of PLA required to implement the following functions? $F(X,Y,Z) = \Sigma m\,(1,3,5,7)$, $G(X,Y,Z) = \Sigma m\,(0,2,4,6)$	(10)
19	(a)	Design a BCD ripple counter using T flipflops	(6)
	(b)	Explain the implementation of full adder using Hardware Description Language (HDL).	(4)
20		Draw and explain the flow chart for addition and subtraction of two binary numbers in sign magnitude form.	(10)

STLQ @P December 2019

① 1111 1111 1111 1111

F F F F

Hexadecimal ⇒ $(FFFF)_{16}$

Decimal

32768 + 16384 + 8192 + 4096 + 2048 + 1024 + 512 + 256 + 128 + 64 + 32 + 16 + 8 + 4 + 2 + 1

1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1

1024
1024
2048
2048
4096
4096
8192
8192
16384
16384
32768

⇒ $(65535)_{10}$.

② 10011 − 10010 Smaller no from bigger.

2's complement

⇒ 01101 +
1
01110

10011 +
01110
100001
Neglect End Around carry.

(ii) 100010 − 100110 bigger from smaller.

2's complement

⇒ 011001 +
1
011010

100010 +
011010
111100

To get original result, take 2's complement.

⇒ 000011 + 1 ⇒ 000100

③ (i) $\overline{x\bar{y} + \bar{x}y}$ by Demorgan's law.

$= \overline{x\bar{y}} \cdot \overline{\bar{x}y} = \bar{x} + y \cdot x + \bar{y}$

$\Rightarrow (\bar{x} + y)(x + \bar{y})$

(ii) $\overline{(a+c)(a+\bar{b})(\bar{a}+b+\bar{c})}$

$(\overline{a+c}) + \overline{(a+\bar{b})} + \overline{(\bar{a}+b+\bar{c})}$

$= \bar{a} \cdot \bar{c} + \bar{a} \cdot b + a \cdot \bar{b} \cdot c$

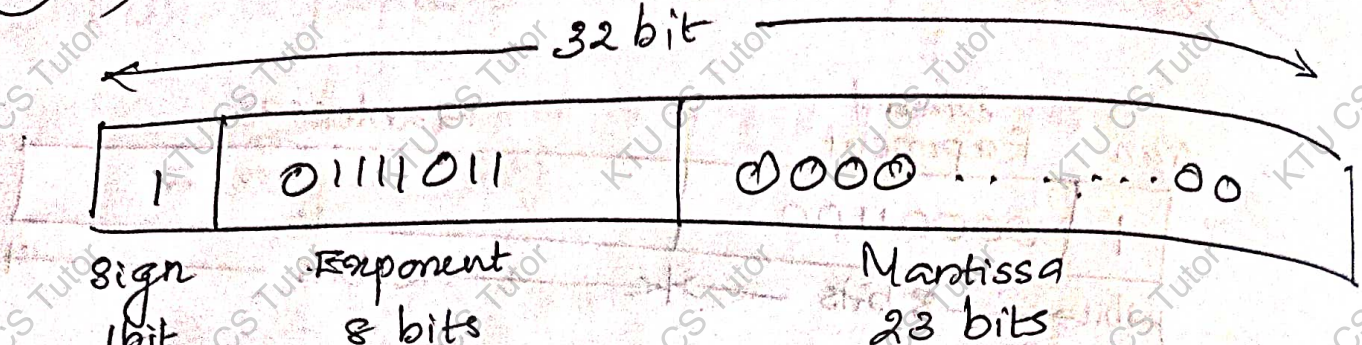
$= \bar{a}\bar{c} + \bar{a}b + a\bar{b}c$

④ Absorption law states that

$x \cdot (x + y) = x$ and

$x + (x \cdot y) = x$.

(5) a) -0.0625



$-0.0625 \Rightarrow$ convert to binary

$0.0625 \times 2 = 0.125 \quad -0$

$0.125 \times 2 = 0.250 \quad -0$ $\qquad (.0001)_2$

$0.25 \times 2 = 0.5 \quad -0$

$0.5 \times 2 = 1.0 \quad \rightarrow 1$

Making first digit as 1 to get normalized form

1.000×2^{-4}

Scientific format

$1.\underbrace{xxxx}_{\text{mantissa}} \times 2^{e}$

Since number is negative,

Sign bit = 1

To get the biased exponent, add the exponent -4 with single precision exponent bias for 32 bit 127

$\Rightarrow 127 + -4 = 123$

Convert to binary $\Rightarrow (1111011)_2$

Make as 8 bits $\Rightarrow$ 01111011 to get exponent

2 | 123
2 | 61 — 1
2 | 30 — 1
2 | 15 — 0
2 | 7 — 1
2 | 3 — 1
1 — 1

Here, our mantissa part is 0.
Represent it in 23 bits.

ABCDEF

(5) b) i) 16's complement of C3DF

Since given number is 4 digit, Subtract this number from the least 5 digit number in hexadecimal.

i.e. 10000 − C3DF

$= (3B21)_{16}$

```
 10000 -
  C3DF
------
  3B21
```

(ii) convert C3DF to binary.

C 3 D F

$(1100\ 0011\ 1101\ 1111)_2$.

(iii) Find the 2's complement of the result in (ii)

1's Complement + 1

```
0011 1100 0010 0000 +
                    1
-------------------
(0011 1100 0010 0001)2
```

(6) a) (i)

```
  1011
+  101
------
 10000
```

$(10000)_2$

```
  1011
x  101
------
  1011
 0000
1011
------
110111
```

$(110111)_2$

(ii) $(62)_8 + (37)_8$

```
  1
  62
+ 37
-----
 121
```

$(121)_8$

$(62)_8 \times (37)_8$

```
   1
  62
x 37
-----
 536
226
-----
3016
```

(iii) $(2E)_{16} + (34)_{16} = (62)_{16}$

```
   1
  2E
+ 34
-----
  62
```

$2E \times 34 =$

$E \times 4 \Rightarrow 14 \times 4 = (56)_{10} \Rightarrow (38)_{16}$

$3 \times E \Rightarrow 3 \times 14 = (42)_{10}$

$\Rightarrow (2A)_{16}$

```
   2
  2E
x 34
-----
 B8
84
-----
958
```

$(958)_{16}$

8 | 14
1 — 6

$7 \times 2 = 14 \Rightarrow 16$

8 | 42
5 — 2

$6 \times 7 = 42 = 52$

$6 \times 3 = 18 \Rightarrow 22$

8 | 18
2 — 2

10 11 12 13 14 15
A B C D E F

16 | 56
3 — 8

16 | 42
2 — 10

⑥ b) 791

$(0111\ 1001\ 0001)_{BCD}$

658

$(0110\ 0101\ 1000)_{BCD}$

```
  0111  1001  0001   +
  0110  0101  1000
-------------------
  1101  1110  1001
  >9    >9
  Add 0110  Add 0110  Add 0

  1101  1110  1001   +
  0110  0110  0000
-------------------
  0001  0100  0100  1001
    1     4     4     9
```

⑦ a) 10110001 AND

(i) 10101100

```
  10100000
```

(ii) 10110001 OR

10101100

```
  10111101
```

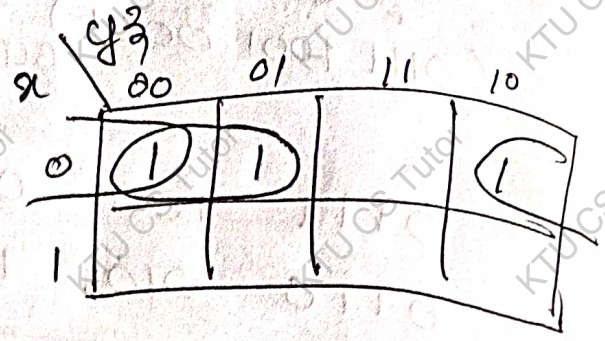
(iii) 10110001 XOR

10101100

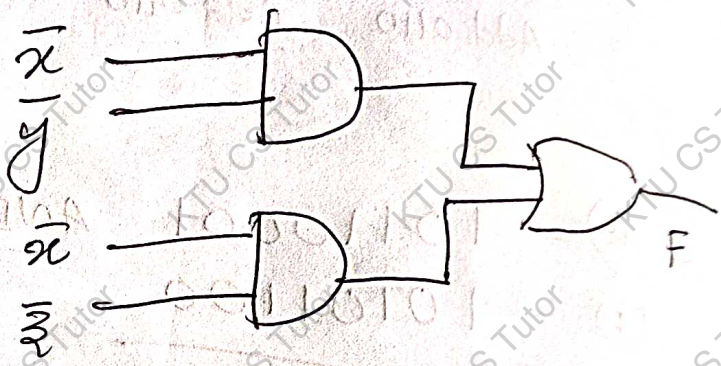
```
  00011101
```

(8)

x	y	z	F
0	0	0	1
0	0	1	1
0	1	0	1
0	1	1	0
1	0	0	0
1	0	1	0
1	1	0	0
1	1	1	0



$F = \bar{x}\bar{y} + \bar{x}\bar{z}$

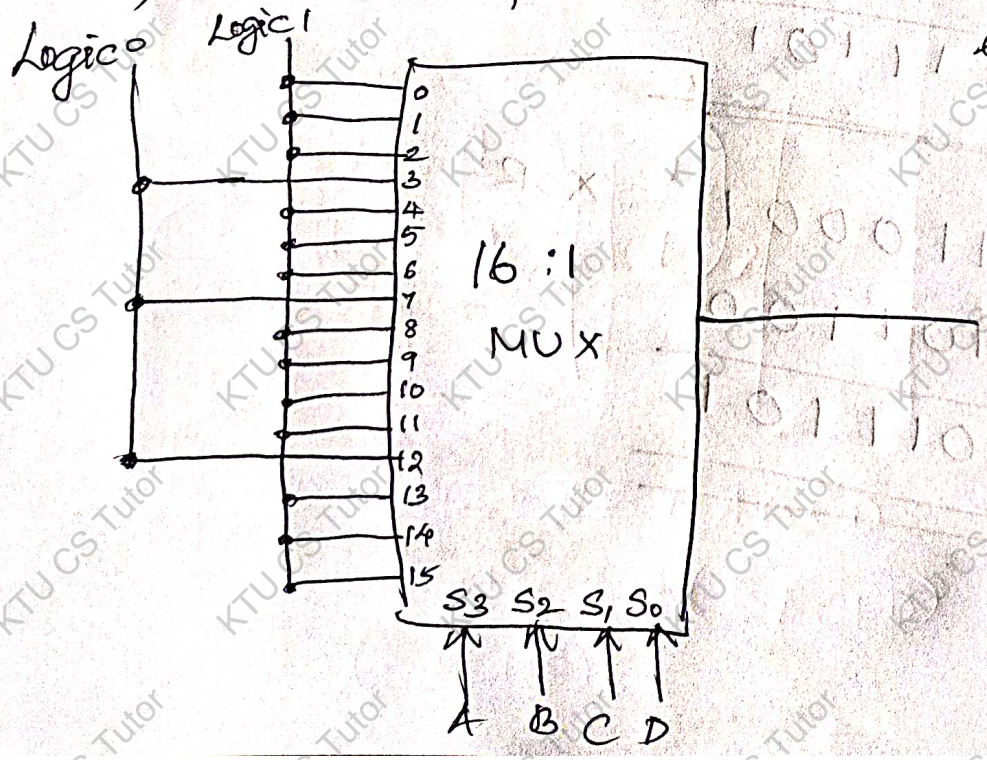


(9) $F(A,B,C,D) = \Pi(3,7,12)$

Since there are 4 variables, 4 select lines in MUX

So, $2^4 = 16$ input lines.

Given Maxterm equivalent O/P should be connected to logic 0 and all others to logic 1

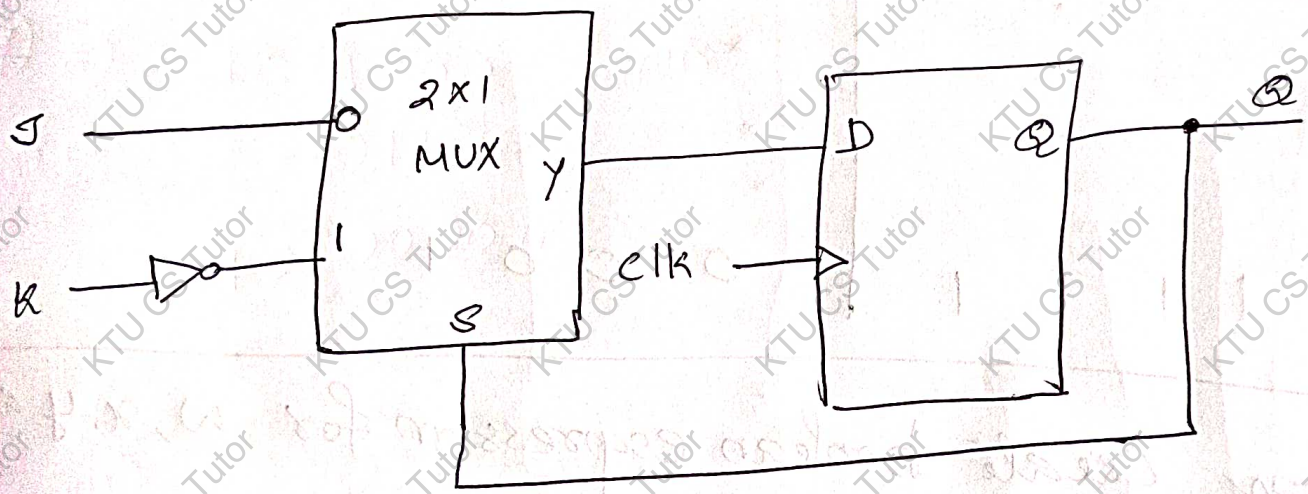


(10) Difference between Combinational and Sequential circuit

eg. Adder, Subtracter, MUX, Decoder etc are combinational

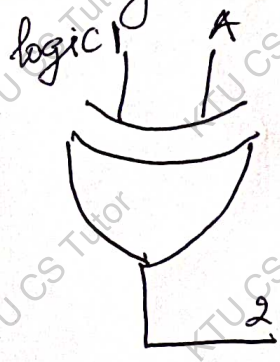
Counters, Shift registers etc are Sequential

(11) JK Flip flop using D Flip flop, 2 to 1 MUX and an inverter.



(12) a) 4 bit 2's complementer using XOR gate.

When a logic 1 is XORed with any i/p, we will get the 2's complement of that i/p.



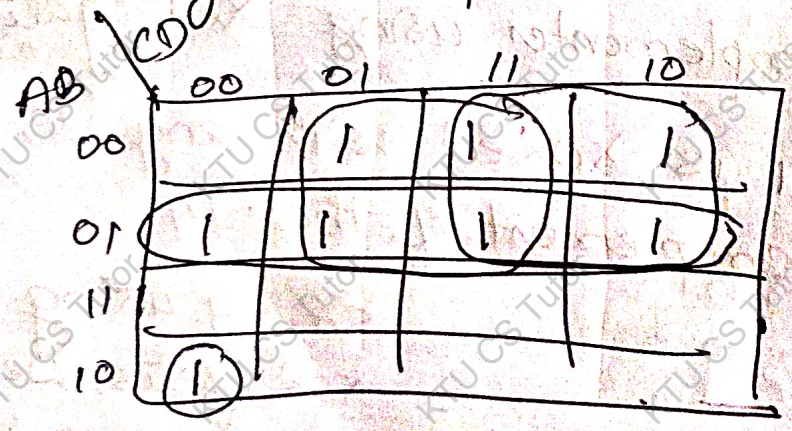
So by using 4 XOR gates, we can construct a 4 bit 2's complementer.

Two bit

To construct the 4 bit 2's complementer, first construct the truth table

A	B	C	D	W	x	y	z
0	0	0	0	0	0	0	0
0	0	0	1	1	1	1	1
0	0	1	0	1	1	1	0
.	.	.	.	.	.	.	.
.	.	.	.	.	.	.	.
.	.	.	.	.	.	.	.
1	1	1	1	0	0	0	1

Then create boolean expression for w, x, y and z using k map.



$x = B \oplus (C+D)$

$y = C \oplus D$

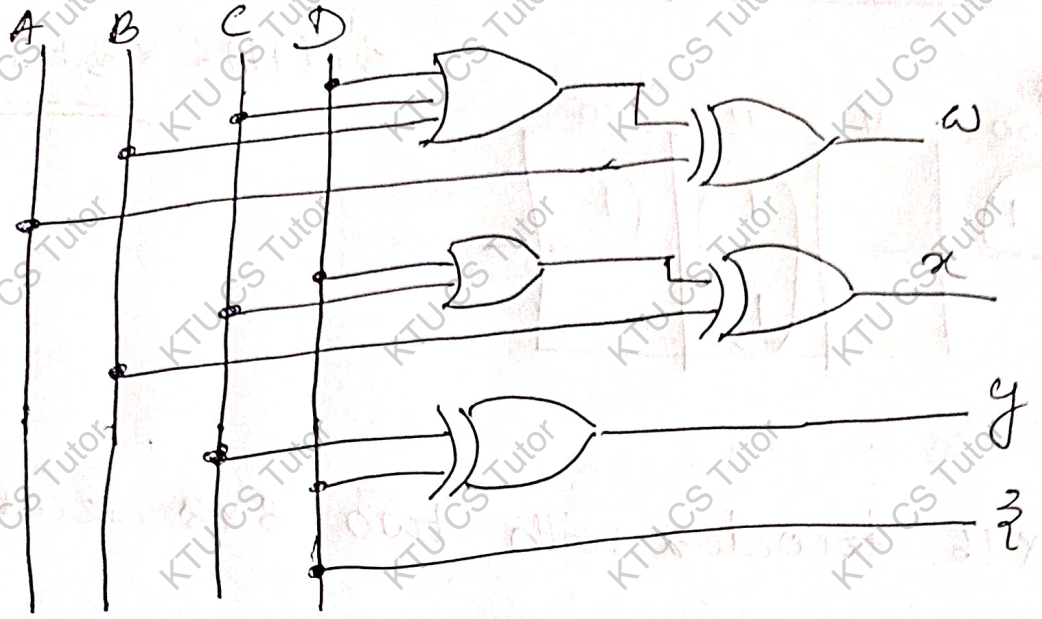
$z = D$

$W = \bar{A}D + \bar{A}C + \bar{A}B + A\bar{B}\bar{C}\bar{D}$

$= \bar{A}(B+C+D) + A\overline{(B+C+D)}$

$= A \oplus (B+C+D)$

Then construct the circuit.



(b) For a 5 bit 2's complementer with MSB = E then the o/p

$$V = E \oplus (A + B + C + D)$$

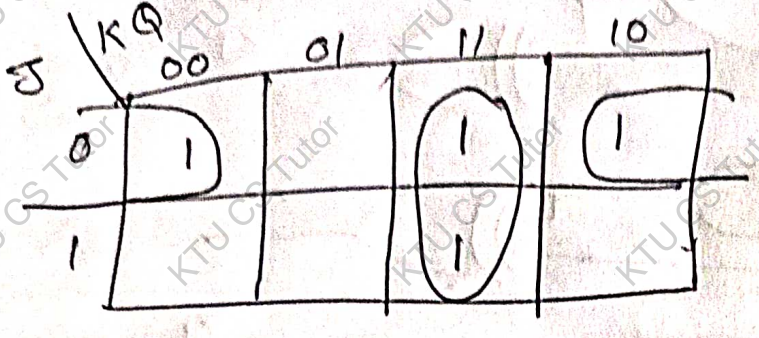
(13) Characteristic eqn of JK FF is

$$Q(t+1) = JQ' + K'Q$$

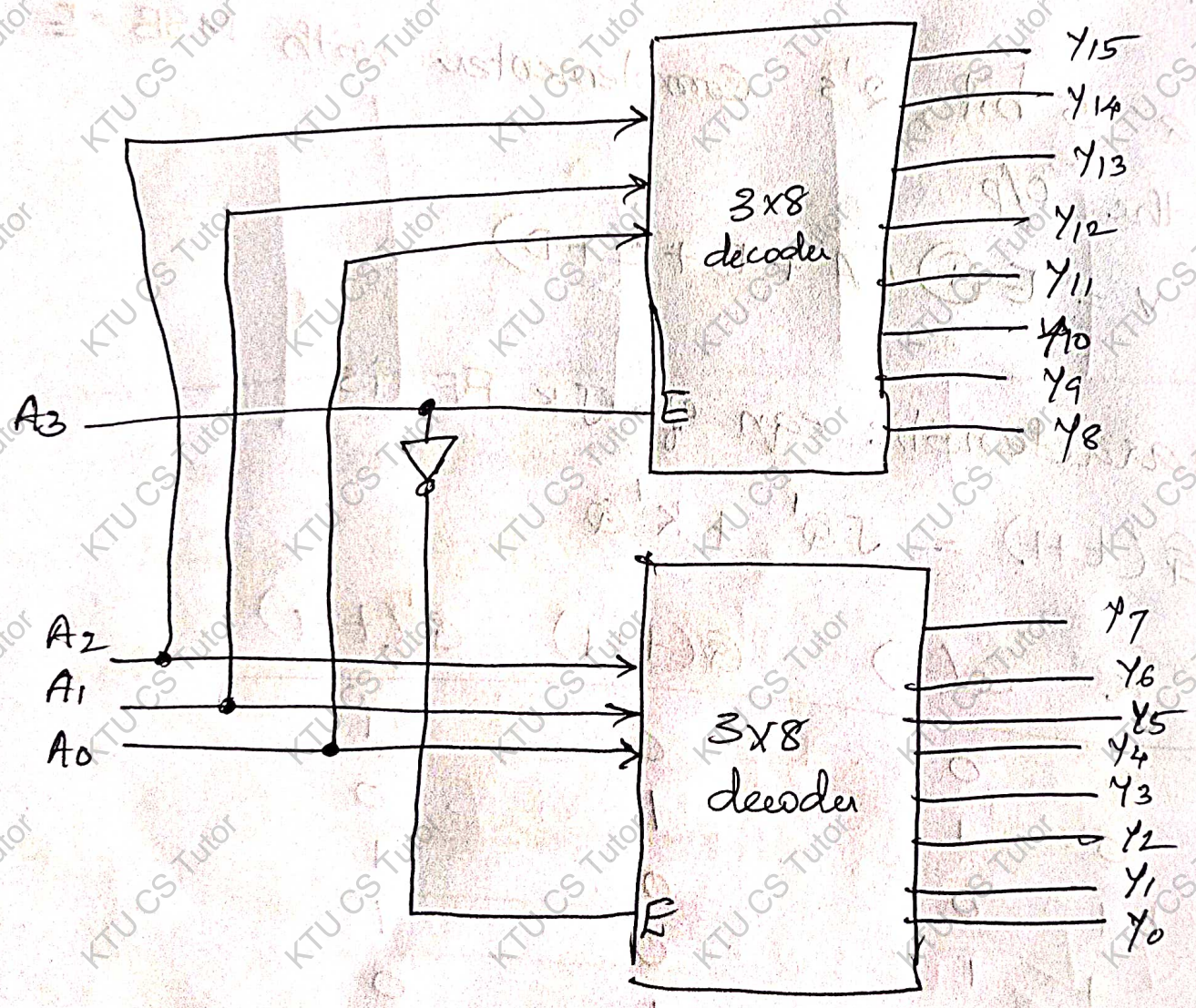
J	K	Q(t)	Q(t+1)	Q'(t+1)
0	0	0	0	1
0	0	1	1	0
0	1	0	0	1
0	1	1	0	1
1	0	0	1	0
1	0	1	1	0
1	1	0	1	0
1	1	1	0	1

K map for $Q'(t+1)$.

$Q'(t+1) = KQ + J'Q'$



(b) 4 x 16 decoder with two 3 x 8 decoders



c) T Flip flop using NAND gates